

LM555/NE555/SA555

Single Timer

Features

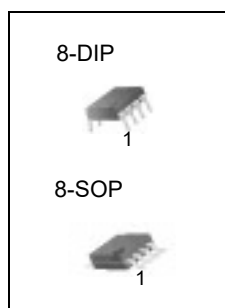
- High Current Drive Capability (200mA)
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From μSec to Hours
- Turn off Time Less Than $2\mu\text{Sec}$

Applications

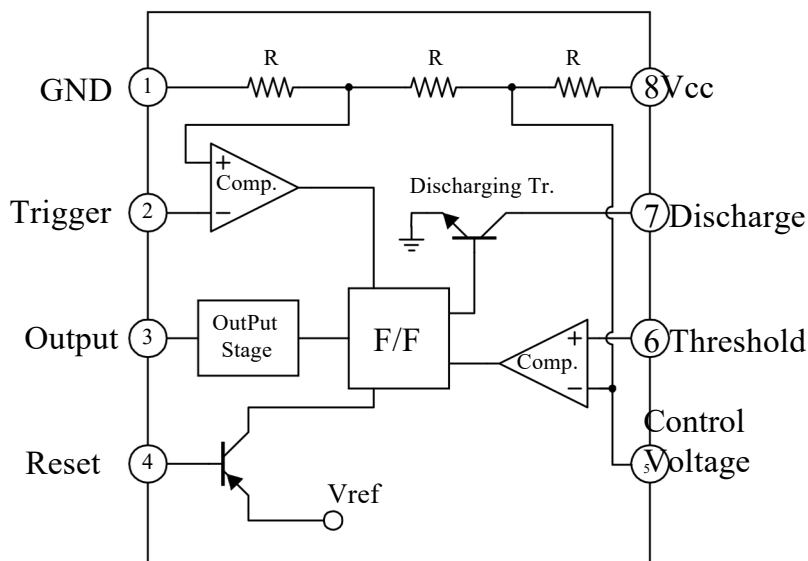
- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing

Description

The LM555/NE555/SA555 is a highly stable controller capable of producing accurate timing pulses. With a monostable operation, the time delay is controlled by one external resistor and one capacitor. With an astable operation, the frequency and duty cycle are accurately controlled by two external resistors and one capacitor.



Internal Block Diagram



AbsoluteMaximumRatings(TA = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	16	V
Lead Temperature (Soldering 10sec)	TLEAD	300	°C
Power Dissipation	PD	600	mW
Operating Temperature Range LM555/NE555 SA555	TOPR TSTG	0 ~ +70 -40 ~ +85	°C
Storage Temperature Range		-65 ~ +150	°C

Electrical Characteristics

(TA = 25°C, VCC = 5 ~ 15V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	-	4.5	-	16	V
Supply Current (Low Stable) (Note1)	ICC	VCC = 5V, RL = ∞	-	3	6	mA
		VCC = 15V, RL = ∞	-	7.5	15	mA
Timing Error (Monostable) Initial Accuracy (Note2) Drift with Temperature (Note4) Drift with Supply Voltage (Note4)	ACCUR $\frac{\Delta t}{\Delta T}$ $\frac{\Delta t}{\Delta V_{CC}}$	RA = 1kΩ to 100kΩ C = 0.1μF	-	1.0 50 0.1	3.0 - 0.5	% ppm/°C %/V
Timing Error (Astable) Initial Accuracy (Note2) Drift with Temperature (Note4) Drift with Supply Voltage (Note4)	ACCUR $\frac{\Delta t}{\Delta T}$ $\frac{\Delta t}{\Delta V_{CC}}$	RA = 1kΩ to 100kΩ C = 0.1μF	-	2.25 150 0.3	-	% ppm/°C %/V
Control Voltage	VC	VCC = 15V	9.0	10.0	11.0	V
Threshold Voltage	VTH	VCC = 5V	2.6	3.33	4.0	V
		VCC = 15V	-	10.0	-	V
Threshold Current (Note3)	ITH	VCC = 5V	-	3.33	-	V
		VCC = 15V	-	10.0	-	V
Trigger Voltage	VTR	VCC = 5V	-	0.1	0.25	μA
		VCC = 15V	1.1	1.67	2.2	V
Trigger Current	ITR	VCC = 5V	4.5	5	5.6	V
		VCC = 15V	4.5	5	5.6	V
Reset Voltage	VRST	VTR = 0V	-	0.01	2.0	μA
Reset Current	IRST	-	0.4	0.7	1.0	V
		-	-	0.1	0.4	mA
Low Output Voltage	VOL	VCC = 15V ISINK = 10mA ISINK = 50mA	-	0.06 0.3 0.05	0.25 0.75	V V V
		VCC = 5V ISINK = 5mA	-	-	0.35	V
High Output Voltage	VOH	VCC = 15V ISO URC = 200mA IE = 100mA	12.75	12.5 13.3	-	V V
		VCC = 5V ISO URC = 100mA	2.75	3.3	-	V
Rise Time of Output (Note4)	tR	-	-	100	-	ns
Fall Time of Output (Note4)	tF	-	-	100	-	ns
Discharge Leakage Current	ILKG	-	-	20	100	nA

Notes:

- When the output is high, the supply current is typically 1mA less than at VCC = 5V.
- Tested at VCC = 5.0V and VCC = 15V.
- This will determine the maximum value of RA + RB for 15V operation, the max. total R = 20MΩ, and for 5V operation, the max. total R = 6.7MΩ.
- These parameters, although guaranteed, are not 100% tested in production.

Application Information

Table 1 below is the basic operating table of 555 timer:

Table 1. Basic Operating Table

Threshold Voltage (Vth)(PIN 6)	Trigger Voltage (Vtr)(PIN 2)	Reset(PIN 4)	Output(PIN 3)	Discharging Tr. (PIN 7)
Don't care	Don't care	Low	Low	ON
$V_{th} > 2V_{cc} / 3$	$V_{th} > 2V_{cc} / 3$	High	Low	ON
$V_{cc} / 3 < V_{th} < 2 V_{cc} / 3$	$V_{cc} / 3 < V_{th} < 2 V_{cc} / 3$	High	-	-
$V_{th} < V_{cc} / 3$	$V_{th} < V_{cc} / 3$	High	High	OFF

When the low signal input is applied to the reset terminal, the timer output remains low regardless of the threshold voltage or the trigger voltage. Only when the high signal is applied to the reset terminal, the timer's output changes according to threshold voltage and trigger voltage.

When the threshold voltage exceeds 2/3 of the supply voltage while the timer output is high, the timer's internal discharge Tr. turns on, lowering the threshold voltage to below 1/3 of the supply voltage. During this time, the timer output is maintained low. Later, if a low signal is applied to the trigger voltage so that it becomes 1/3 of the supply voltage, the timer's internal discharge Tr. turns off, increasing the threshold voltage and driving the timer output again at high.

1.Monostable Operation

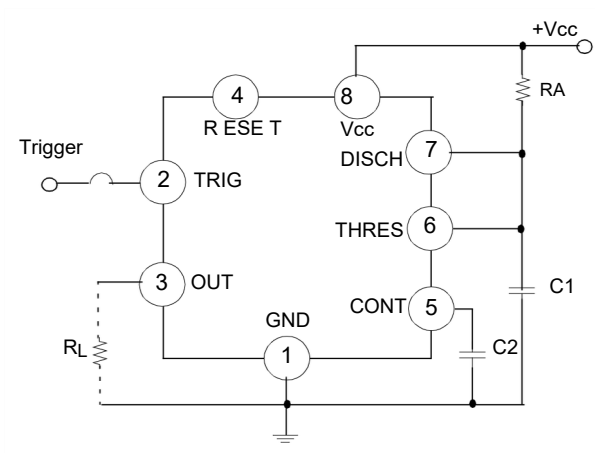


Figure 1. Monoatable Circuit

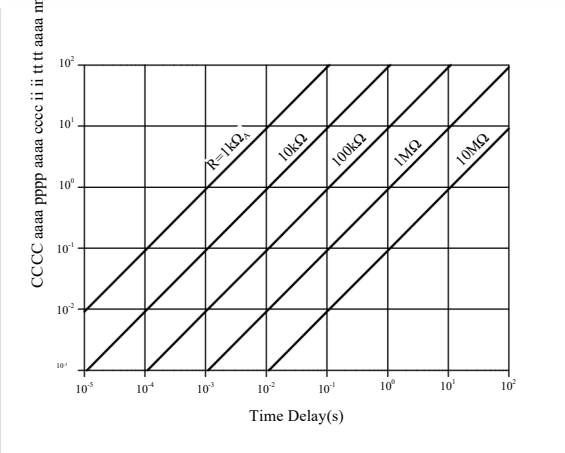


Figure 2. Resistance and Capacitance vs. Time delay(td)

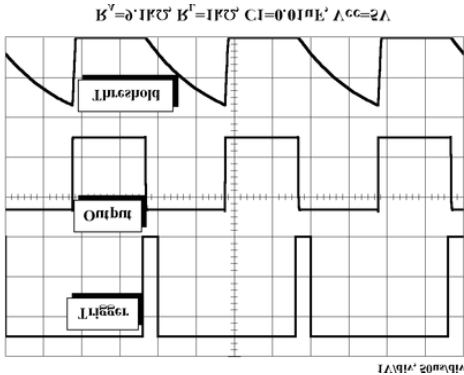


Figure 3. Waveforms of Monostable Operation

Figure 1 illustrates a monostable circuit. In this mode, the timer generates a fixed pulse whenever the trigger voltage falls below $V_{CC}/3$. When the trigger pulse voltage applied to the #2 pin falls below $V_{CC}/3$ while the timer output is low, the timer's internal flip-flop turns the discharging Tr. off and causes the timer output to become high by charging the external capacitor C1 and setting the flip-flop output at the same time.

The voltage across the external capacitor C1, VC1 increases exponentially with the time constant $t = RA * C$ and reaches $2V_{CC}/3$ at $t_d = 1.1RA * C$. Hence, capacitor C1 is charged through resistor RA. The greater the time constant RAC, the longer it takes for the VC1 to reach $2V_{CC}/3$. In other words, the time constant RAC controls the output pulse width.

When the applied voltage to the capacitor C1 reaches $2V_{CC}/3$, the comparator on the trigger terminal resets the flip-flop, turning the discharging Tr. on. At this time, C1 begins to discharge and the timer output converts to low.

In this way, the timer operating in the monostable repeats the above process. Figure 2 shows the time constant relationship based on RA and C. Figure 3 shows the general waveforms during the monostable operation.

It must be noted that, for a normal operation, the trigger pulse voltage needs to maintain a minimum of $V_{CC}/3$ before the timer output turns low. That is, although the output remains unaffected even if a different trigger pulse is applied while the output is high, it may be affected and the waveform does not operate properly if the trigger pulse voltage at the end of the output pulse remains at below $V_{CC}/3$. Figure 4 shows such a timer output abnormality.

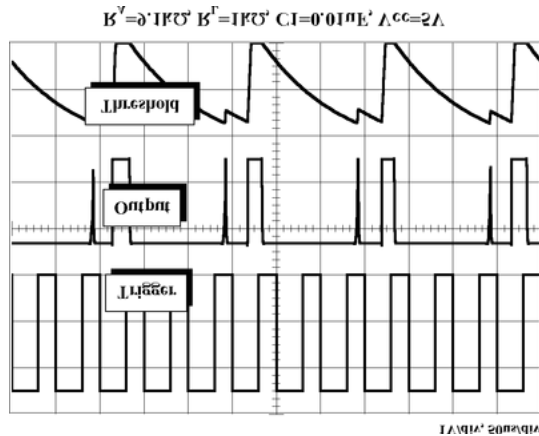


Figure4. Waveforms of Monostable Operation (abnormal)

2. Astable Operation

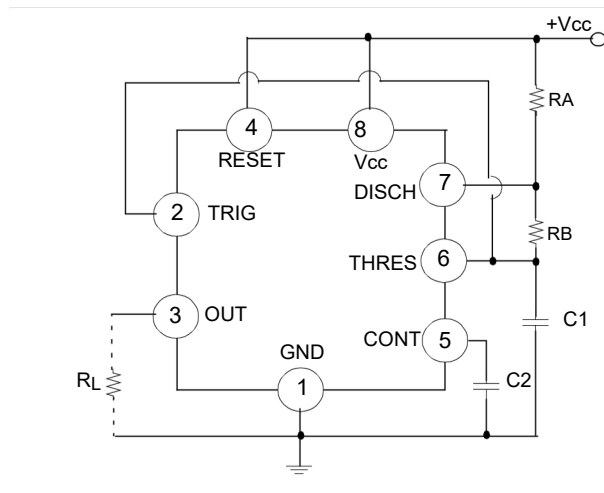


Figure 5. Astable Circuit

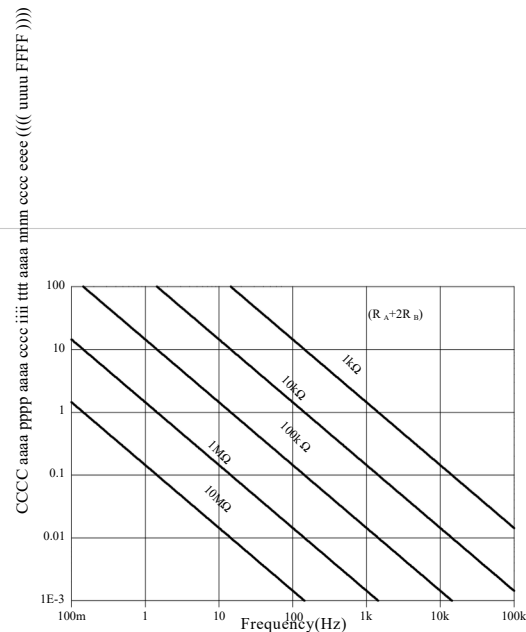


Figure 6. Capacitance and Resistance vs. Frequency

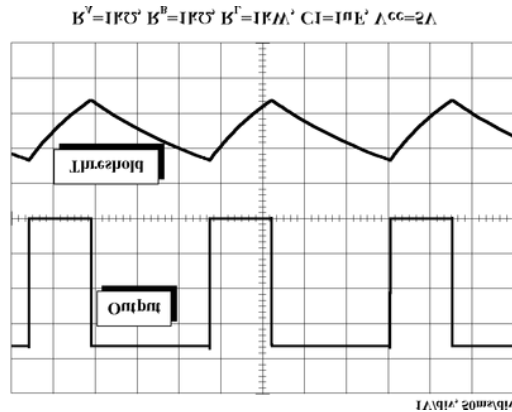
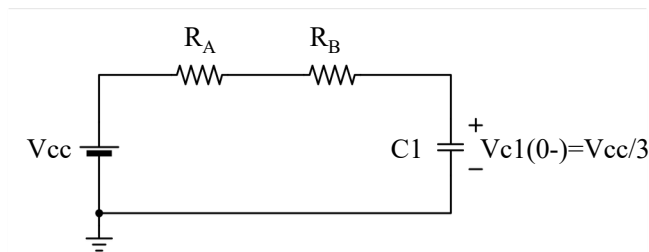


Figure7. Waveforms of Astable Operation

An astable timer operation is achieved by adding resistor R_B to Figure 1 and configuring as shown on Figure 5. In the astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a multi vibrator. When the timer output is high, its internal discharging Tr turns off and the $VC1$ increases by exponential function with the time constant $(R_A + R_B) \cdot C$.

When the $VC1$, or the threshold voltage, reaches $2V_{CC}/3$, the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This in turn turns on the discharging Tr and the $C1$ discharges through the discharging channel formed by R_B and the discharging Tr . When the $VC1$ falls below $V_{CC}/3$, the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging Tr turns off and the $VC1$ rises again.

In the above process, the section where the timer output is high is the time it takes for the $VC1$ to rise from $V_{CC}/3$ to $2V_{CC}/3$, and the section where the timer output is low is the time it takes for the $VC1$ to drop from $2V_{CC}/3$ to $V_{CC}/3$. When timer output is high, the equivalent circuit for charging capacitor $C1$ is as follows:



$$C_1 \frac{dV_{C1}}{dt} = \frac{V_{CC} - V(0-)}{R_A + R_B} \quad (1)$$

$$V_{C1}(0+) = V_{CC}/3 \quad (2)$$

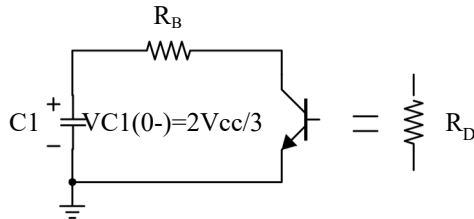
$$V_{C1}(t) = V_{CC} \left[\frac{1}{3} - \frac{2}{3} e^{-\frac{t}{(R_A + R_B)C_1}} \right] \quad (3)$$

Since the duration of the timer output high state (t_H) is the amount of time it takes for the $V_{C1}(t)$ to reach $2V_{CC}/3$,

$$V_{C1}(t) = -2V_{CC} = V_{CC} \left(1 - 2e^{-\frac{t}{(R_A + R_B)C_1}} \right) \quad (4)$$

$$t_H = C_1(R_A + R_B) \ln 2 = 0.693(R_A + R_B)C_1 \quad (5)$$

The equivalent circuit for discharging capacitor C_1 , when timer output is low is, as follows:



$$C_1 \frac{dv}{dt} = -\frac{V_{C1}}{R_B + R_D} \quad (6)$$

$$V_{C1}(t) = -3V_{CC} e^{-\frac{t}{(R_A + R_D)C_1}} \quad (7)$$

Since the duration of the timer output low state (t_L) is the amount of time it takes for the $V_{C1}(t)$ to reach $V_{CC}/3$,

$$\frac{V_{CC}}{3} = -3V_{CC} e^{-\frac{t}{(R_A + R_D)C_1}} \quad (8)$$

$$t_L = C_1(R_B + R_D) \ln 2 = 0.693(R_B + R_D)C_1 \quad (9)$$

Since R_D is normally $R_D \gg R_B$ although related to the size of discharging T_r , $t_L \approx 0.693R_D C_1$ (10)

Consequently, if the timer operates in astable, the period is the same with $T = t_H + t_L = 0.693(R_A + R_B)C_1 + 0.693R_D C_1 = 0.693(R_A + 2R_B)C_1$ because the period is the sum of the charge time and discharge time. And since frequency is the reciprocal of the period, the following applies.

$$\text{frequency, } f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1} \quad (11)$$

3. Frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 1 can be made to operate as a frequency divider. Figure 8. illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

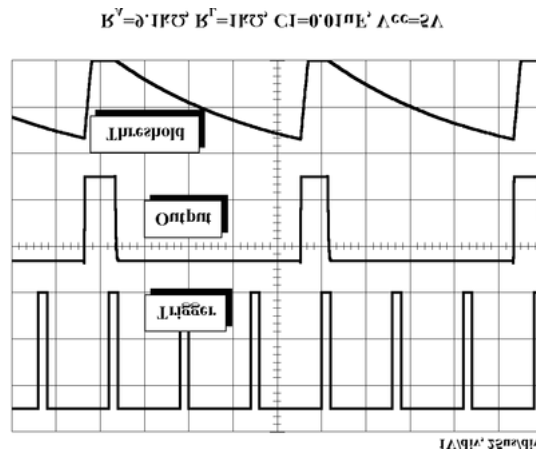


Figure 8. Waveforms of Frequency Divider Operation

4. Pulse Width Modulation

The timer output waveform may be changed by modulating the control voltage applied to the timer's pin 5 and changing the reference of the timer's internal comparators. Figure 9 illustrates the pulse width modulation circuit.

When the continuous trigger pulse train is applied in the monostable mode, the timer output width is modulated according to the signal applied to the control terminal. Sine wave as well as other waveforms may be applied as a signal to the control terminal. Figure 10 shows the example of pulse width modulation waveform.

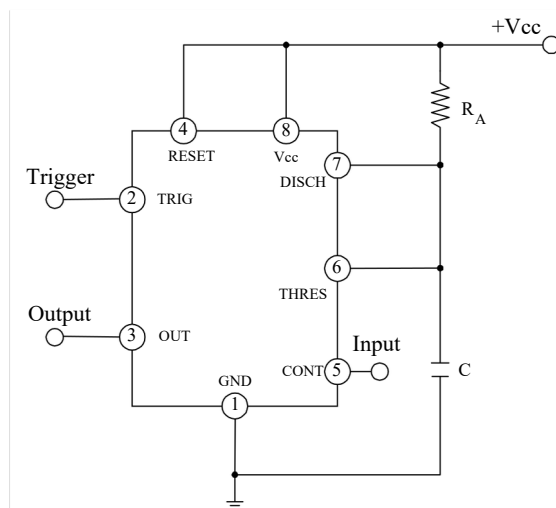


Figure 9. Circuit for Pulse Width Modulation

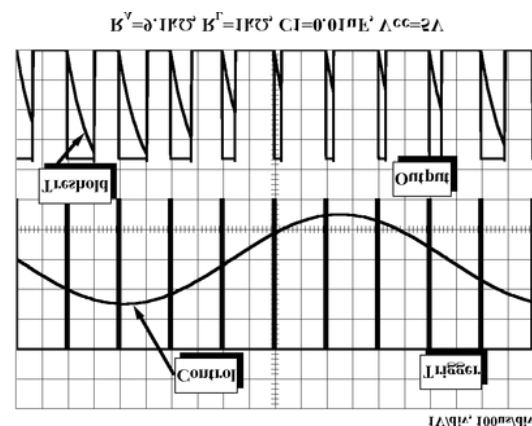


Figure 10. Waveforms of Pulse Width Modulation

5. Pulse Position Modulation

If the modulating signal is applied to the control terminal while the timer is connected for the astable operation as in Figure 11, the timer becomes a pulse position modulator.

In the pulse position modulator, the reference of the timer's internal comparators is modulated which in turn modulates the timer output according to the modulation signal applied to the control terminal.

Figure 12 illustrates a sine wave for modulation signal and the resulting output pulse position modulation : however, any wave shape could be used.

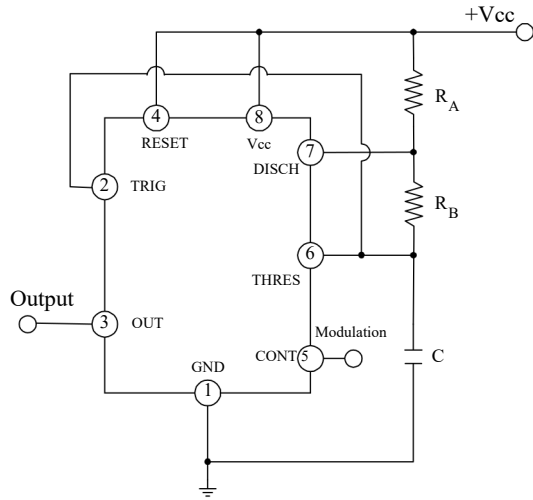


Figure 11. Circuit for Pulse Position Modulation

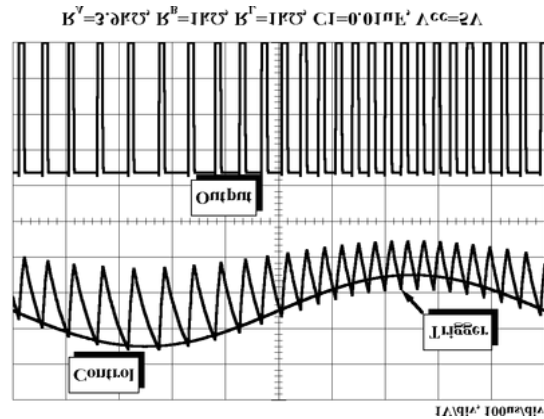


Figure 12. Waveforms of pulse position modulation

6. Linear Ramp

When the pull-up resistor R_A in the monostable circuit shown in Figure 1 is replaced with constant current source, the VC1 increases linearly, generating a linear ramp. Figure 13 shows the linear ramp generating circuit and Figure 14 illustrates the generated linear ramp waveforms.

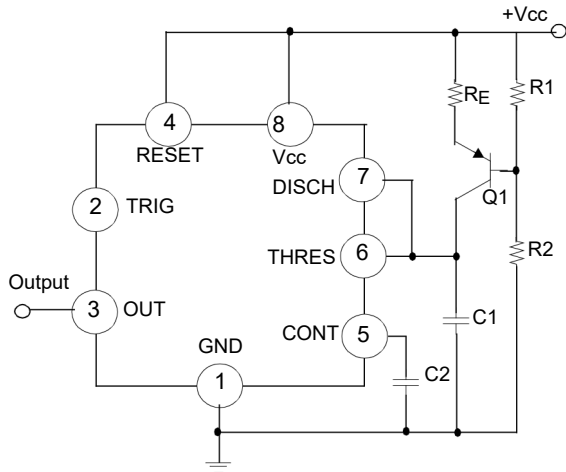


Figure13.CircuitforLinearRamp

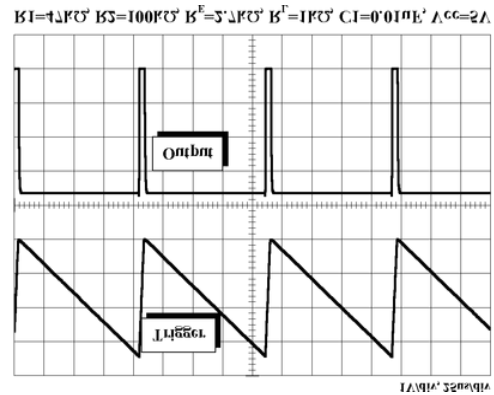


Figure14.Waveformsof Linear Ramp

In Figure 13, current source is created by PNP transistor Q1 and resistor R1, R2, and RE.

$$I_C = \frac{V_{CC} - V_{BE}}{R_E} \quad (12)$$

Here, V_{BE} is

$$V_E = V_{BE} + \frac{R_2}{R_1 + 2} V_{CC} \quad (13)$$

For example, if $V_{CC}=15V$, $R_E=20k\Omega$, $R_1=5k\Omega$, $R_2=10k\Omega$, and $V_{BE}=0.7V$,

$$V_E = 0.7V + 10V = 10.7V$$

$$I_C = (15 - 10.7) / 20k = 0.215mA$$

When the trigger starts in a timer configured as shown in Figure 13, the current flowing through capacitor C1 becomes a constant current generated by PNP transistor and resistors.

Hence, the V_C is a linear ramp function as shown in Figure 14. The gradient S of the linear ramp function is defined as follows:

$$S = \frac{V_{p-p}}{T} \quad (14)$$

Here the V_{p-p} is the peak-to-peak voltage.

If the electric charge amount accumulated in the capacitor is divided by the capacitance, the V_C comes out as follows:

$$V = Q/C \quad (15)$$

The above equation divided on both sides by T gives us

$$\frac{V}{T} = \frac{Q}{C} \quad (16)$$

and may be simplified into the following equation.

$$S = I/C \quad (17)$$

In other words, the gradient of the linear ramp function appearing across the capacitor can be obtained by using the constant current flowing through the capacitor.

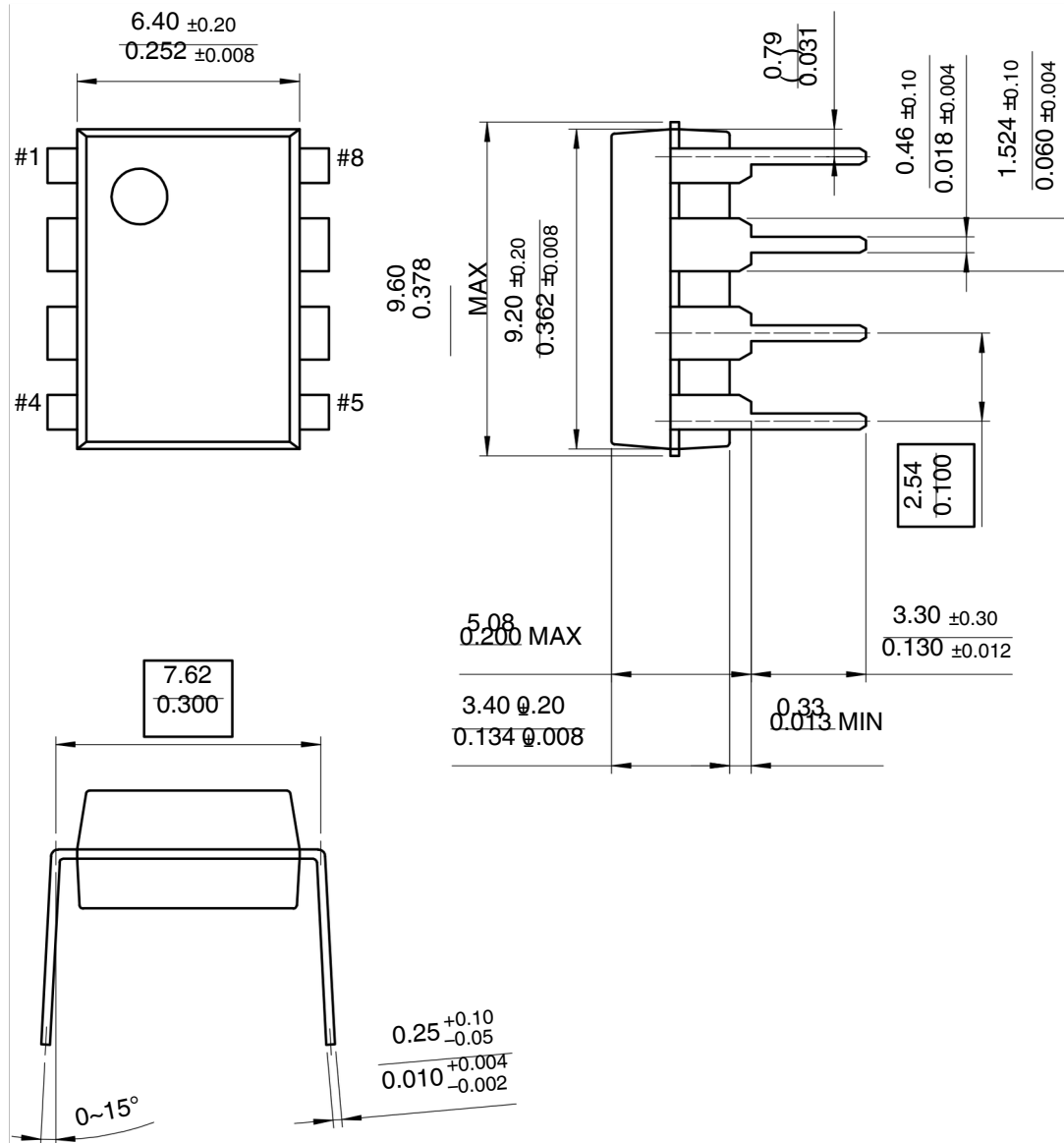
If the constant current flow through the capacitor is 0.215mA and the capacitance is 0.02 μ F, the gradient of the ramp function at both ends of the capacitor is $S = 0.215\text{m}/0.022\mu = 9.77\text{V/ms}$.

Mechanical Dimensions

Package

Dimensions in millimeters

8-DIP



Ordering Information

Product Number	Package	Operating Temperature
LM555CN	8-DIP	0 ~ +70°C
LM555CM	8-SOP	
Product Number	Package	Operating Temperature
NE555N	8-DIP	0 ~ +70°C
NE555D	8-SOP	
Product Number	Package	Operating Temperature
SA555	8-DIP	-40 ~ +85°C
SA555D	8-SOP	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems

which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support

device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.